CLAIMS

We claim:

1. A control method of an MRAM (Magnetoresistive Random Access Memory) based on vertical current writing, characterized in that the writing operation of information in a magnetic film cell MFC of the MRAM is implemented by corporate effect of magnetic fields generated by a current parallel to the MFC and another current vertical to the MFC and passing through this MFC.

2. An MRAM based on vertical current writing, comprising:
a) a memory control unit array composed of transistor ATR (4) units, the control unit array being integrated in a semiconductor substrate;
b) a memory cell array composed of a magnetic film cell MFC (2);
c) contact holes (3e, 3f) and a transitional metal layer, the magnetic film cell MFC (2) being connected to the transistor ATR (4) units through the contact holes (3e, 3f) and the transitional metal layer; and
d) a word line WL (3d) and a bit line BL (3a),
characterized in that the bit line BL (3a) being arranged above on the magnetic film cell MFC (2), directly connected with the magnetic film cell MFC (2), and vertical to an easy magnetization direction of the magnetic film cell MFC (2).

3. The MRAM based on vertical current writing according to claim 2, wherein a current-limiting mechanism is arranged which can be constituted by a diode and/or a transistor, and one or more current-limiting mechanisms are connected to each bit line BL and are arranged in a peripheral circuit of the MRAM array.

4. The MRAM based on vertical current writing according to claim 3, wherein the basic structure of the magnetic film cell MFC (2) is constituted by two magnetic material layers and a nonmagnetic material layer interposed between the two magnetic material layers, and stored information is represented and stored by the magnetization state of one of the magnetic material layers.

5. The MRAM based on vertical current writing according to claim 4, wherein the bit line BL (3a) and the word line WL (3d) are vertical to each other, and the easy magnetization direction of the magnetic film cell MFC (2) is vertical to the bit line BL (3a).

6. The MRAM based on the vertical current writing according to claim 5, wherein the word line WL (3d) also acts as the gate of the transistor ATR (4) unit.

7. The MRAM based on vertical current writing according to claim 6, wherein, in the process of reading information, the transistor ATR (4) is turned on and a read current is introduced from the bit line BL (3a) so as to obtain the information stored in the magnetic film cell MFC (2).

8. The MRAM based on the vertical current writing according to any of claims 2-7, wherein there are altogether two internal metal wiring layers, i.e., a layer (5d) where the bit line BL (3a) locates and a layer (5b) where the transitional metal layer (3b) and the ground line GND (3c) locate.

9. An MRAM (Magnetoresistive Random Access Memory) based on vertical current writing, comprising:

a) a memory read/write control unit array composed of transistor ATR (4) units, the read/write control unit being integrated in a semiconductor substrate;

b) a memory cell array composed of a magnetic film cell MFC (2);

c) contact holes (3e, 3f); and

d) a word line WL (3d) and two bit lines BL1 (3a) and BL2 (3g),

characterized in that further comprising a transitional metal layer (3b), the magnetic film cell MFC (2) is connected to the transistor ATR (4) unit through the transitional metal layer (3b) and the contact hole (3f); the bit lines BL1 (3a) and BL2 (3g) are isolated by insulation medium and are parallel to each other in direction, and meantime the bit line BL2 (3g) is connected directly to the magnetic film cell MFC (2).

10. The MRAM based on the vertical current writing according to claim 9, wherein the basic structure of the magnetic film cell MFC (2) is constituted by two magnetic material layers and a nonmagnetic material layer interposed between the two magnetic material layers, and the stored information is represented and stored by the magnetization state of one of the magnetic material layers.

11. The MRAM based on vertical current writing according to claim 10, wherein the directions of the bit lines BL1 (3a) and BL2 (3g) are vertical to an easy magnetization direction of the magnetic film cell MFC (2), and are vertical to the direction of the word line WL (3d).

12. The MRAM based on the vertical current writing according to claim 11, wherein the word

line WL (3d) also acts as the gate of the transistor ATR (4) unit.

13. The MRAM based on vertical current writing according to claim 12, wherein, in the process of reading information, the transistor ATR (4) unit is turned on and a read current is introduced from the bit line BL2 (3g) so as to obtain the information stored in the magnetic film cell MFC (2).

14. The MRAM based on the vertical current writing according to claim 13, wherein the process of its writing operation is implemented by corporate effect of a current parallel to the magnetic film cell MFC (2) on the bit line BL1 (3a) and a current introduced from the bit line BL2 (3g), vertical to the magnetic film cell MFC (2) and passing through the magnetic film cell MFC (2).

15. The MRAM based on vertical current writing according to any of claims 9-14, wherein there are altogether three internal metal wiring layers, i.e., a layer where the bit line BL (3a) locates, a layer where the bit line BL (3g) locates and a layer where the transitional metal layer (3b) and the ground line GND (3c) locate.

16. An MRAM (Magnetoresistive Random Access Memory) based on vertical current writing, comprising:
a) a memory read/write control unit array composed of transistor ATR (4) units, the read/write control unit array being integrated in a semiconductor substrate;
b) a memory cell array composed of a magnetic film cell MFC (2);
c) contact holes (3e, 3f); and
d) two word lines WL1 (3d) and WL2 (3g) and a bit line BL (3a),
characterized in that the word line WL2 (3g) being connected directly to the magnetic film cell MFC (2) and is vertical to the bit line BL (3a).

17. The MRAM based on the vertical current writing according to claim 16, wherein the basic structure of the magnetic film cell MFC (2) is constituted by two magnetic material layers and a nonmagnetic material layer interposed between the two magnetic material layers, and the stored information is represented and stored by the magnetization state of one of the magnetic material layers.

18. The MRAM based on vertical current writing according to claim 17, wherein the bit line BL (3a) is vertical to an easy magnetization direction of the magnetic film cell MFC (2), and is vertical to the word lines WL1 (3d) and WL2 (3g).

19. The MRAM based on the vertical current writing according to claim 18, wherein the bit line BL (3a) is arranged above on the word line WL2 (3g) and is isolated from it by insulation.

20. The MRAM based on the vertical current writing according to claim 19, wherein the word line WL (3d) also acts as the gate of the transistor ATR (4) unit.

21. The MRAM based on the vertical current writing according to claim 20, wherein, in the process of reading information, the transistor ATR (4) is turned on and a read current is introduced from the word line WL2 (3g) so as to obtain the information stored in the magnetic film cell MFC (2).

22. The MRAM based on the vertical current writing according to claim 21, further comprising a transitional metal layer (3b), the magnetic film cell MFC (2) being connected to the transistor ATR (4) unit through the transitional metal layer (3b) and the contact hole (3f).

23. The MRAM based on the vertical current writing according to claim 22, wherein the process of its writing operation is implemented by corporate effect of a current parallel to the magnetic film cell MFC (2) on the bit line BL (3a) and a current introduced from the word line WL2 (3g), vertical to the magnetic film cell MFC (2) and passing through the magnetic film cell MFC (2).

24. The MRAM based on vertical current writing according to any of claims 16-23, wherein there are altogether three internal metal wiring layers, i.e., a layer where the bit line BL (3a) locates, a layer where the word line WL2 (3g) locates and a layer where the transitional metal layer (3b) and the ground line GND (3c) locate.